AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions or listing of claims for this application:

Listing of Claims:

Claims 1-8 (Canceled).

9. (Currently amended) A semiconductor apparatus formed on a semiconductor substrate having a first conductivity type, comprising:

an internal circuit formed on the semiconductor substrate;

a plurality of external connection terminals formed in a first portion of said semiconductor substrate around said internal circuit, said external connection terminals being electrically connected to said internal circuit, wherein a plurality of power supply voltages are provided to said external connection terminals; and

one or more outer ESD elements formed in a second portion of said semiconductor substrate or in a common well region in said semiconductor substrate, around the first portion of said semiconductor substrate;

wherein each of said one or more outer ESD elements further comprises:

a first terminal electrically connected between a first diffusion region and ~~to~~ a higher voltage level of a main power supply;

a second terminal electrically connected between a second diffusion region and ~~to~~ a lower voltage level of the main power supply; and

a third terminal electrically connected between a third diffusion region and ~~to~~ said external connection terminals, said first, second and third diffusion regions being formed separately from each other on said substrate, said third diffusion region causing

electrostatic noise to be discharged through one of said first and second diffusion regions.

10. (new) The semiconductor apparatus of claim 9, further comprising a gate electrode between said third terminal and said third diffusion region.

11. (new) The semiconductor apparatus of claim 10, wherein said third diffusion region is located between said first and second diffusion regions, said first and third diffusion regions forming a first transistor and said second and third diffusion regions forming a second transistor.

12. (new) The semiconductor apparatus of claim 9 further comprising a plurality of outer ESD protective circuits.